Homework #9: ECE 461/661

PID, Meeting Specs, Delays. Due Monday, October 28th
20 points per problem

PID:

A 3rd-order model for the following 10-stage RC filter is

$$G(s) = \left(\frac{2331}{(s+2.6338)(s+30.2062)(s+53.7896)} \right)$$

I Compensation

1) Design an I compensator, , which results in 20% overshoot for a step input. For this K(s), determine

- The closed-loop dominant pole(s)
- The 2% settling time,
- The error constant, Kp, and
- The steady-state error for a step input.

Check your design in Matlab or Simulink or VisSim

Give an op-amp circuit to implement K(s)

PI Compensation

2) Design a PI compensator, , which results in 20% overshoot for a step input. For this K(s), determine

- The closed-loop dominant pole(s)
- The 2% settling time,
- The error constant, Kp, and
- The steady-state error for a step input.

Check your design in Matlab or Simulink or VisSim

Give an op-amp circuit to implement K(s)

Meeting Design Specs

3) Design a compensator, K(s), that results in

- No error for a step input
- A 2% settling time of 1 second, and
- 20% overshoot for the step response

Check your design in Matlab or Simulink or VisSim

Give an op-amp circuit to implement K(s)

Systems with Delays

4) Assume a 100ms delay is added to the system

$$G(s) = \left(\frac{2331}{(s+2.6338)(s+30.2062)(s+53.7896)} \right) e^{-0.1s}$$

Design a compensator, K(s), that results in

- No error for a step input
- A 2% settling time of 1 second, and
- 20% overshoot for the step response

Check your design in Matlab or Simulink or VisSim

Give an op-amp circuit to implement K(s)